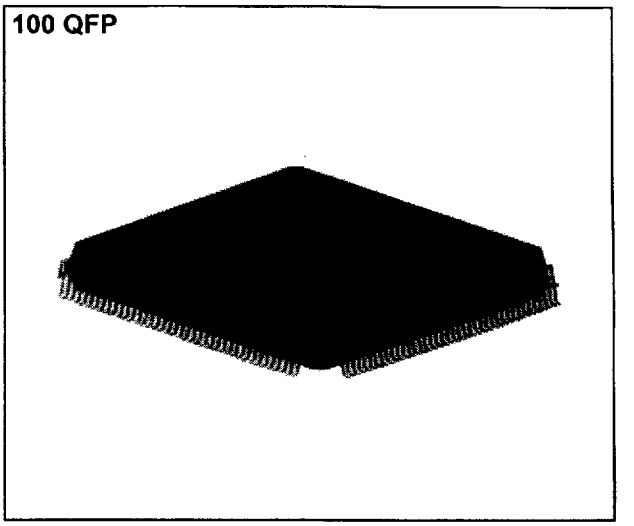
ΩmniWave™ SYNTHESIZER

The **KS0164 ΩmniWave** wavetable synthesizer chip represents the state-of-the-art in multimedia audio technology. **ΩmniWave** combines a high-quality 32-voice wavetable synthesizer, a powerful 16-bit CPU, and MPU-401 compatibility into a single chip. The audio performance of a typical **ΩmniWave** system compares favorably to the best multimedia wavetable solutions available today, but at very low cost. A typical **ΩmniWave** system provides 32 voices of 16-bit, 44.1 KHz sample rate wavetable synthesis, MPU-401 compatibility, General MIDI, GS and MT-32 compatibility. With **ΩmniWave,** a complete wavetable synthesizer may be implemented with as few as three ICs. Both serial and parallel MIDI interfaces are provided.



FEATURES

- **High-quality 32-voice wavetable synthesizer**
- **General MIDI compliant**
- **Three serial output channels for addition of optional audio effects processor**
- **Supports all common CDP D/A formats**
- **Supports up to 24Mbytes of sample memory**
- **Supports 8-bit, 16-bit and compressed samples**
- **Directly supports ROM, SRAM and DRAM**
- **16-bit embedded CPU minimizes host PC overhead**
- **Integrated MIDI UART**
- **Integrated SRAM for embedded CPU**
- **4-pole resonant digital filters**
- **Software-controlled SLEEP mode**
- **Stand-alone mode for use without host PC**
- **Sequoia Development Group synthesizer firmware**

ORDERING INFORMATION

Device	Package	Temperature Range
KS0164	100 QFP	0°~+70°C

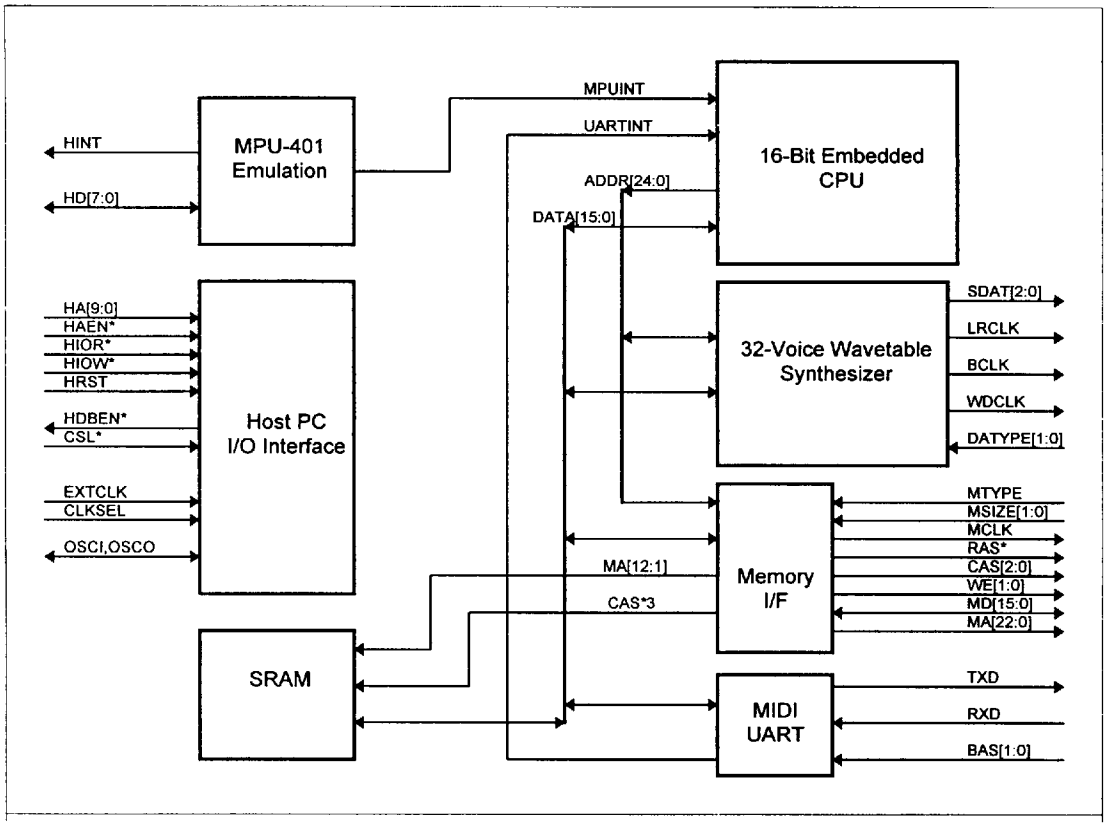
APPLICATIONS

- **MULTIMEDIA AUDIO PRODUCTS**
- **MUSICAL SYNTHESIZERS**
- **VIDEO GAME SOUND SYSTEMS**

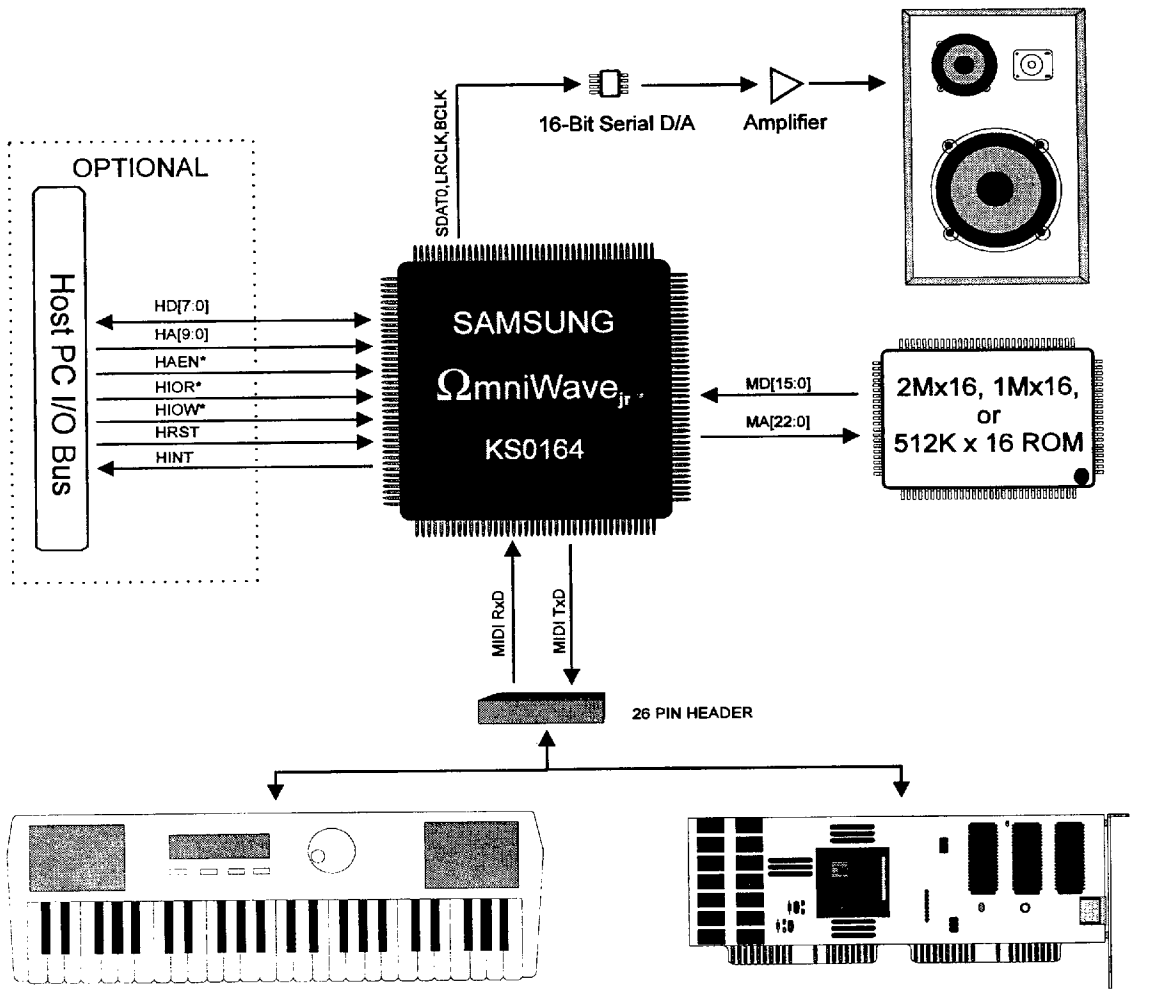
RELATED PRODUCTS

- **KS0174-1M 1MB ΩmniWave Sample ROM**
- **KS0174-2M 2MB ΩmniWave Sample ROM**
- **KS0174-4M 4MB ΩmniWave Sample ROM**
- **KF353/D/S Dual Operational Amplifier**

BLOCK DIAGRAM

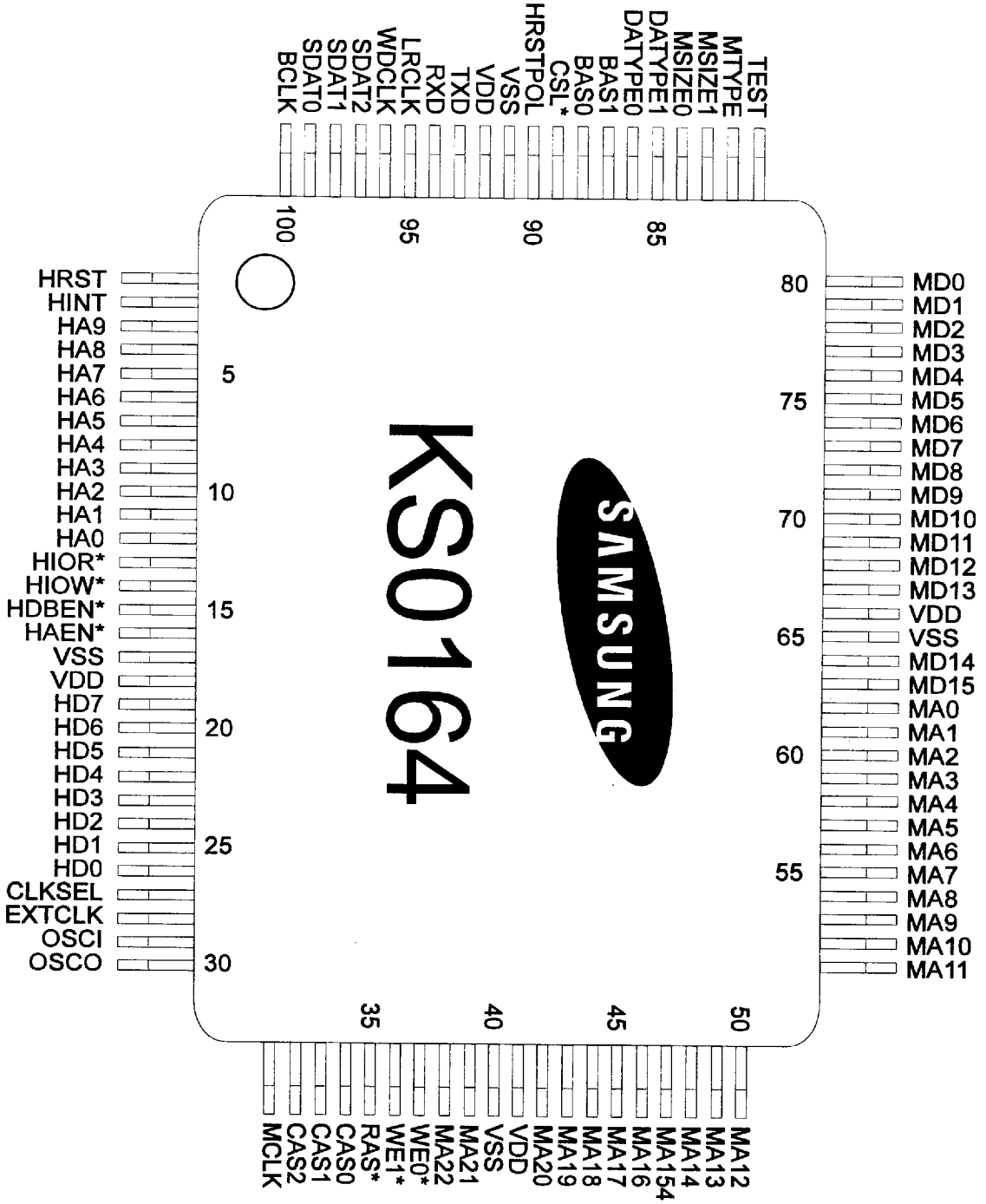


TYPICAL APPLICATION



MIDI Keyboard/Synthesizer/Drum Machine
Or Connection to Sound Card

PIN ASSIGNMENT - 100 QFP



Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	HRST	26	HD0	51	MA11	76	MD4
2	HINT	27	CLKSEL	52	MA10	77	MD3
3	HA9	28	EXTCLK	53	MA9	78	MD2
4	HA8	29	OSCI	54	MA8	79	MD1
5	HA7	30	OSCO	55	MA7	80	MD0
6	HA6	31	MCLK	56	MA6	81	TEST
7	HA5	32	CAS2	57	MA5	82	MTYPE
8	HA4	33	CAS1	58	MA4	83	MSIZE1
9	HA3	34	CAS0	59	MA3	84	MSIZE0
10	HA2	35	RAS*	60	MA2	85	DATYPE1
11	HA1	36	WE1*	61	MA1	86	DATYPE0
12	HA0	37	WE0*	62	MA0	87	BAS1
13	HIOR*	38	MA22	63	MD15	88	BAS0
14	HIOW*	39	MA21	64	MD14	89	CSL*
15	HDBEN*	40	VSS	65	VSS	90	HRSTPOL
16	HAEN*	41	VDD	66	VDD	91	VSS
17	VSS	42	MA20	67	MD13	92	VDD
18	VDD	43	MA19	68	MD12	93	TXD
19	HD7	44	MA18	69	MD11	94	RXD
20	HD6	45	MA17	70	MD10	95	LRCLK
21	HD5	46	MA16	71	MD9	96	WDCLK
22	HD4	47	MA15	72	MD8	97	SDAT2
23	HD3	48	MA14	73	MD7	98	SDAT1
24	HD2	49	MA13	74	MD6	99	SDAT0
25	HD1	50	MA12	75	MD5	100	BCLK

PIN DESCRIPTION

Pin Name	Pin #	Type	Description
HOST PC INTERFACE			
HA[9:0]	3..12	I	Host Address Bits [9:0] These are the low 10 bits of the Host PC address bus, which are decoded to control access to the MPU-401. For PC applications, these pins should be connected directly to A[9:0]. Alternatively, these pins may be tied to VSS, and a fully qualified chip select signal may be connected to the CSL* pin instead.
HAEN*	16	I	Host Address Enable. This is the Host PC I/O enable. All I/O operations are ignored any time this signal is high. For PC applications, these pins should be connected directly to AEN*.
HD[7:0]	19..26	I/O	Buffered Host PC Data Bus Bits [0:7]. These pins have 18mA drivers, so they may be directly connected to the host PC data bus in most applications. If additional buffering is desired a 74LS245 may be used with its Enable pin connected to HDBEN*, and its DIR pin connected to HIOR*.
HIOR*	13	I	Host I/O Read. This is the Host PC I/O read enable.
HIOW*	14	I	Host I/O Write. This is the Host PC I/O write strobe. Data is written to internal registers on the rising edge of this signal.
CSL*	89	I	Chip Select. In most applications where the MPU-401 emulation is being used, the KS0164 address decoder will be used. However, if a non-standard address decode is required, or of a plug-n-play address decode is available, a fully qualified, active-low chip select signal may be connected to this pin instead. If this pin is not used, it must be pulled up to VDD.
HRST	1	I	Host PC Reset. The active polarity of this pin is programmable via the HRSTPOL pin. For PC application, this pin should be connected directly to the PC-bus RSTDRV signal. For daughter card applications, connect this pin to the reset signal from the host board.
HRSTPOL	90	I	Determines the signal polarity of the HRST pin. Set this pin low to make HRST active low (typical for daughter card applications), set this pin high to make HRST active high (use for ISA bus applications).
HINT	2	O	Host MPU-401 Interrupt. This is an active high interrupt output to the Host PC. It should be connected to one of the Host IRQ lines, normally IRQ2.
HDBEN*	15	O	Host PC Data Bus Buffer Enable. This output controls the enable to the 74LS245 which buffers the Host PC data bus. This pin is driven low any time the MPU-401 is addressed for an I/O access.
MEMORY INTERFACE			
MA[22:0]	38..39, 42..62	O	Memory Address Bus Bits [22:0]. This is the external memory address bus. When accessing static memory devices (ROM/SRAM), these pins will contain a stable address throughout the entire memory cycle. When accessing dynamic memory, pins MA[11:0] will contain the multiplexed DRAM address.
MD[15:0]	63..64, 67..80	I/O	Memory Data Bus Bit [15:0]. This is the external memory data bus.
WE1*	36	O	Memory Upper Byte Write Enable. When this signal is low during an external memory access, it indicates that data bits MD[15:8] should be written to the addressed memory device.
WE0*	37	O	Memory Lower Byte Write Enable. When this signal is low during an external memory access, it indicates that data bits MD[7:0] should be written to the addressed memory device.

RAS*	35	O	Dynamic Memory Row Address Strobe. This signal is the Row Address Strobe for all external DRAM. When a DRAM device is addressed, this signal will be driven low shortly after the row address has been placed on MA[11:0]. It will also be driven low during ROM/SRAM cycles to provide CAS-before-RAS refresh for any DRAM devices in the system.
CAS[2:0]*	32..34	O	Dynamic Memory Column Address Strobes/Static Memory Chip Selects [2:0]. When a DRAM device is addressed, one of these signals will be driven low shortly after the column address has been placed on MA[11:0]. It will also be driven low during ROM/SRAM cycles to provide CAS-before-RAS refresh for any DRAM devices in the system. When a ROM or SRAM device is addressed, one of these signals will be driven low shortly after the address has been placed on MA[22:0].
MCLK	31	O	Memory Clock. CPU and synthesizer external memory accesses are 1:1 interleaved. This signal indicates which device currently has control of the memory bus. When low, the CPU has control of the memory bus, when high, the synthesizer has control of the memory bus.
MTYPE	82	I	Memory Type Select. When this pin is tied to VSS, the optional memory device(s) connected to CAS1 and/or CAS2 are configured as static(ROM or SRAM) devices. When this pin is pulled up to VDD, the optional memory device(s) connected to CAS1 and/or CAS2 are configured as dynamic (DRAM) devices.
MSIZE[1:0]	83..84	I	Dynamic Memory Size Select. When optional dynamic memory is connected to CAS1 and/or CAS2, these pins configure the size of the DRAM devices so that proper address multiplexing can be performed by the KS0164. The size is configured as follows: MSIZE1 / MSIZE0 / DRAM Size 0 / 0 / 64K 0 / 1 / 256K 1 / 0 / 1M 1 / 1 / 4M

CLOCK INPUT

OSCI	29	I	16.9344 MHz Oscillator Buffer Input. This input will normally be connected to one side of a 16.9344MHz crystal, with a 20pF capacitor to ground. If desired, an externally generated 16.9344MHz clock may be connected to this pin instead. Note that due to internal analog circuitry, the chip may not behave reliably if this clock input is not close to the design frequency.
OSCO	30	O	16.9344 MHz Oscillator Buffer Out. This input will normally be connected to one side of a 16.9344MHz crystal, with a 20pF capacitor to ground. If the OSCI pin is being driven by an externally generated clock, this pin should be left unconnected.
EXTCLK	28	I	External Clock Input. This input may be used to make use of an externally generated clock in place of the on-chip oscillator. This clock may be of any frequency up to 33MHz.
CLKSEL	27	I	External Clock Select. When this pin is low, the on-chip oscillator is disabled, and EXTCLK is used as the clock source for all on-chip timing. When high, the on-chip oscillator is enabled.

D/A & EFFECTS PROCESSOR INTERFACE

SDAT[2:0]	97..99	O	D/A Converter Serial Data [2:0]. These are the three serial data outputs from the synthesizer core. Three outputs are provided so that one "dry" channel, and two separate effects channels can be provided by an external audio effects processor. In a minimum configuration, with no effects external processor, SDAT0 would be connected to the data input of an external 16-bit stereo serial D/A converter, while SDAT[1:2] would be left unconnected.
BCLK	100	O	D/A Converter Bit Clock. This is the bit clock for the external serial D/A converter for the synthesizer.
WDCLK	96	O	D/A Converter Word Clock. This is the word clock for the external serial D/A Converter for the synthesizer.
LRCLK	95	O	D/A Converter L/R Clock. This is the L/R clock for the external serial D/A converter for the synthesizer.
DATYPE[1:0]	85..86	I	D/A Converter Type Select. These pins select the interface type for the D/A converter. Four different standard interfaces are supported as follows: DATYPE1 / DATYPE0 / D/A Data Format 0 / 0 / 32-bit Frame, 1 BCLK Delay (I2S) 0 / 1 / 32-bit Frame, No Delay 1 / 0 / 64-bit Frame, Left-Justified 1 / 1 / 64-bit Frame, Right-Justified (Japanese)

MISCELLANEOUS

RXD	94	I	MIDI Receive Data. This is the TTL-level serial input to the 31.25 kBAUD MIDI UART. For normal MIDI communication, this pin must be driven by an external opto-isolator from the current-loop MIDI line.
TXD	93	O	TTL MIDI Transmit Data. This is the TTL-level serial output from the 31.25 kBAUD MIDI UART. For normal MIDI communication, this pin must drive an external voltage-to-current converter to drive the current-loop MIDI line.
BAS[1:0]	87..88	I	MPU-401 Base Address Select [1:0]. These pins select whether the MPU-401 emulation will be decoded at address 320H, 330H, 340H, or 350H. BAS1 / BAS0 / ADDRESS 0 / 0 / 320H 0 / 1 / 330H 1 / 0 / 340H 1 / 1 / 350H
TEST	81		TEST Pin - Manufacturing Test Pin. For normal operation, this pin must be tied to GND. Applying power to the device with this pin floating or tied to a logic high level may cause permanent damage to the device.

POWER AND GROUND

VDD	18,41,66,92	+5V	Digital power supply.
VSS	17,40,65,91	GND	Digital ground.

GENERAL DESCRIPTION

The **KS0164 ΩmniWave** is a highly integrated wavetable synthesizer chip, designed to be part of high-performance, low-cost multimedia audio systems. The chip contains a complete 32-voice, 16-bit, 44.1kHz wavetable synthesizer, a high-performance 16-bit CPU, compatibility with established standard audio interfaces, and all necessary system glue logic. With its on-chip CPU, an **ΩmniWave**-based synthesizer imposes absolutely minimal host CPU overhead. Its hardware-based MPU-401 emulation completely eliminates the memory overhead, software compatibility, and stability problems of TSR-based emulations. The following sections give a brief description of the major functional blocks of the KS0164.

HOST PC INTERFACE

All necessary ISA bus interface logic is completely contained on-chip. This includes address decoding for the MPU-401 emulation, control signal interpretation, and optional data bus buffer control. All PC interface control logic operates completely asynchronously to the synthesizer/CPU logic. Standard interfacing techniques are used to provide a highly compatible and reliable interface.

The MPU-401 emulation can be decoded for any one of four standard address ranges, as selected by the BAS[1:0] pins. In addition, a serial MIDI interface may be used, leaving the MPU-401 emulation inactive. This mode is particularly useful for stand-alone synthesizer modules and WaveBlaster-type daughter board applications.

To better support non-PC-based applications, including stand-alone applications where no host CPU is available, the reset signal polarity is programmable via the HRSTPOL pin, to accomodate existing active high or active low reset signals.

MPU-401 INTERFACE

One of the two available interfaces for communicating MIDI data to/from the KS0164 is the on-chip MPU-401 emulation. This emulation provides the full hardware functionality of a real MPU-401. MPU-401 UART mode is fully supported, while a subset of the "intelligent" mode commands are also supported. The intelligent-mode support currently provided is adequate to support nearly all existing MPU-401 applications.

MIDI UART INTERFACE

The second of the two available interfaces for communicating MIDI data to/from the KS0164 is the on-chip of MIDI UART. This interface is always active, and works independantly from the MPU-401 emulation, allowing the KS0164 to easily be used in stand-alone MIDI modules and WaveBlaster-type daughter board applications.

EMBEDDED CPU

In sharp contrast to many other low-cost multimedia audio solutions currently available, the KS0164 does not rely on the host PC processor or a slow external microcontroller to drive the wavetable synthesizer. Rather, the KS0164 contains a high-performance custom-built 16-bit CPU incorporating such advanced features as six different addressing modes, a hardware multiplier, a barrel shifter, and a peak execution rate of nearly 3 million instructions per second. In addition to providing optimal synthesizer audio quality, this reduces host PC CPU overhead and the resulting degradation of application/game performance. The considerable memory overhead, compatibility problems, and erratic audio quality associated with TSR-based solutions are also completely eliminated.

SYNTHESIZER

The synthesizer is a high-performance 32-voice, 16-bit wavetable synthesizer. While nearly all wavetable systems being offered today operate at sample rates ranging anywhere from 22-32kHz, the KS0164 performs all sample processing at a full 44.1 kHz. In addition, some other systems support only 12-bit samples. The KS0164, on the other hand, supports 8- and 16-bit linear samples, and 8- and 12-bit compressed samples. This allows nearly optimal tradeoffs between sample size and audio quality on a sample-by-sample basis in the design of the sample set, resulting in the best possible sound quality from a given total sample memory size.

The specifications for the synthesizer are as follows:

Architecture:	Digital Wavetable Synthesizer
Voices:	32
Polyphony:	32 Notes Maximum
Multi-Timbral Capability:	Up To 16 Parts
Sample Memory:	Up To 24 M bytes of ROM/SRAM/DRAM
Available Sample Sets:	2Mx16-bits, 1Mx16-bits, 512Kx16-bits
D/A Converter:	16-Bit Linear Serial Converter, All Common Data Formats Supported
Sample Playback Rate:	Fixed @ 44.1 kHz
Level And Panning Controls:	Separate 16-Bit L&R Volume Controls For Each Voice
Filters:	2 Separate 2-Pole Resonant Digital Filters For Each Voice
Data Formats:	8- Or 16-Bit Signed Linear Or 8- Or 12-Bit Compressed
Envelopes:	Hardware Envelopes For Amplitude and Filters
Effects:	Effects Loop Provided For optional DSP Multiple Effects Processor
Firmware:	Sequoia Development Group Pegasus Synthesizer Firmware
Compatibility:	Fully General-MIDI Compliant Roland MT-32 Sound Set Compatible

SYSTEM TIMING AND CONTROL

All timing is derived from a 16.9344 MHz crystal oscillator, or an externally generated oscillator of any frequency up to 33Mhz. However, note that the internal MIDI UART baud rate is directly proportional to the system clock rate. At any crystal frequency other than 16.9344 Mhz, the UART BAUD rate will not be correct.

SAMPLE MEMORY INTERFACE

Each memory access cycle consists of 3 cycles of the 16.9344 MHz master clock, or 177.15 nSec. This is adequate to allow use of 150 nS ROM, and 80 nSec DRAM. The memory interface supports a minimum of one and a maximum of three memory devices. The device connected to CAS0 must be a ROM. In general the CPU will execute entirely out of this ROM, and most, if not all, synthesizer voices will also be playing primarily from this ROM, although entirely RAM-based systems can be supported with some additional logic. ROM memory accesses are exploited to allow DRAM refresh to occur simultaneously with ROM accesses by executing CAS-before-RAS refresh cycles on all DRAM banks in parallel with all ROM/SRAM accesses.

DIRECT-ADDRESSED REGISTERS

MPU-401 DATA REGISTER — **READ/WRITE**

ADDRESS	MNEMONIC	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BASE+0	HMD	D7	D6	D5	D4	D3	D2	D1	D0

D[7:0] MPU-401 data.

MPU-401 COMMAND REGISTER — **WRITE ONLY**

ADDRESS	MNEMONIC	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BASE+1	HMC	C7	C6	C5	C4	C3	C2	C1	C0

C[7:0] MPU-401 command.

MPU-401 STATUS REGISTER — **READ ONLY**

ADDRESS	MNEMONIC	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BASE+1	HMC	RXRDY	TXRDY	1	1	1	1	1	1

RXRDY Received Data Ready Status

0 = Received data is available in HMD
1 = Received data is not available

TXRDY Transmit Data Buffer Ready Status

0 = MPU-401 is ready to receive next data/command in HMD or HMC
1 = MPU-401 is not ready to receive next data/command

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	MIN	MAX	UNIT
Supply Voltage (Measured To V_{ss})	V_{DD}	-0.5	+7.0	V
Input Voltage (Any Pin)	V_{IN}	V_{SS}-0.5	V_{DD}+0.5	V
Ambient Operating Temperature Range	T_{opr}	0	+70	°C
Storage Temperature Range	T_{stg}	-55	+150	°C

Notes:
1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions is not implied.

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage (Measured To V_{SS})	V_{DD}	4.75	5.0	+5.25	V
Digital Input High Voltage	V_{IH}	2.2	-	V_{DD}+0.3	V
Digital Input Low Voltage	V_{IL}	V_{SS}-0.3	-	0.8	V
Digital Output High Voltage (I_{oh}=400μA)	V_{OH}	2.4	-	-	V
Digital Output Low Voltage (I_{ol}=3.2mA)	V_{OL}	-	-	0.45	V
Input Leakage High Current	I_{IH}	-10	0	10	μA
Input Leakage Low Current*	I_{IL}	-10	0	10	μA
Supply Current	I_{CC}	-	100	250	mA
Pull-up Resistance**	R_{UP}	40		250	kΩ

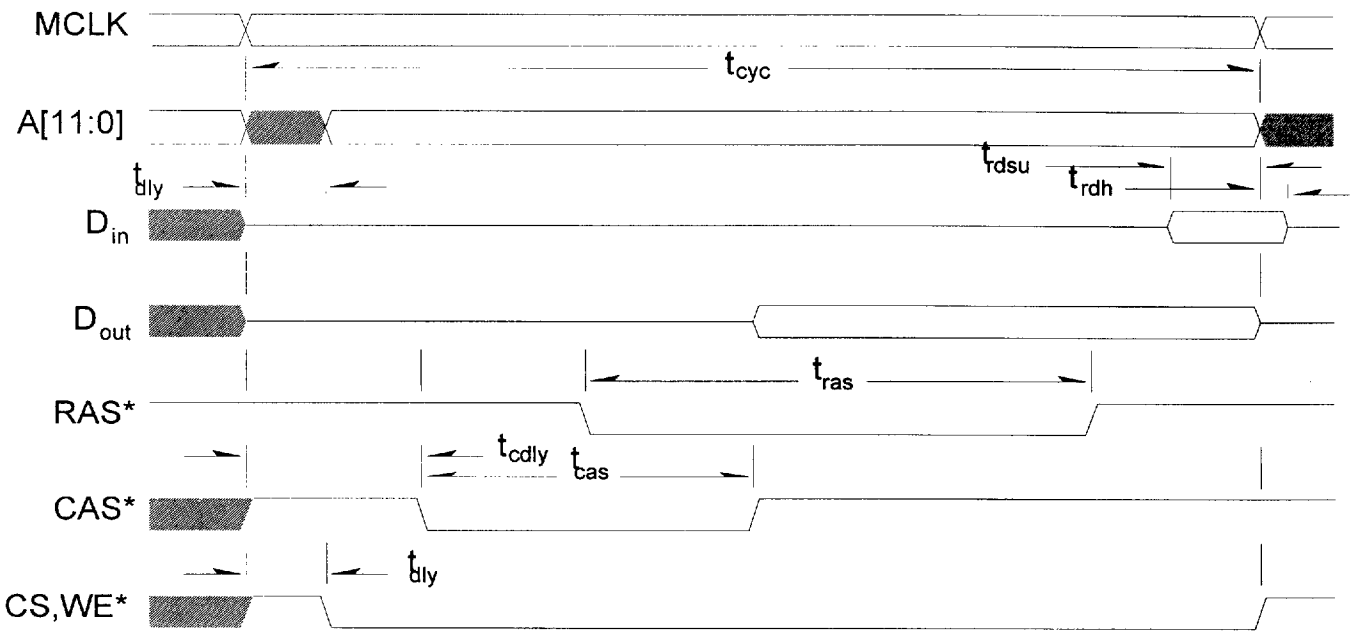
Notes:
1. Test Condition: V_{DD}=5.0V, V_{SS}=0V, f_{OSC}=16.9344MHz, T_a=25°C.
2. * For pins TEST, MTYPE, MSIZE1-0, BAS1-0, HRSTPOL, HRST, DATYPE1-0, and CSL.
3. ** All input pins except * above.

AC ELECTRICAL CHARACTERISTICS

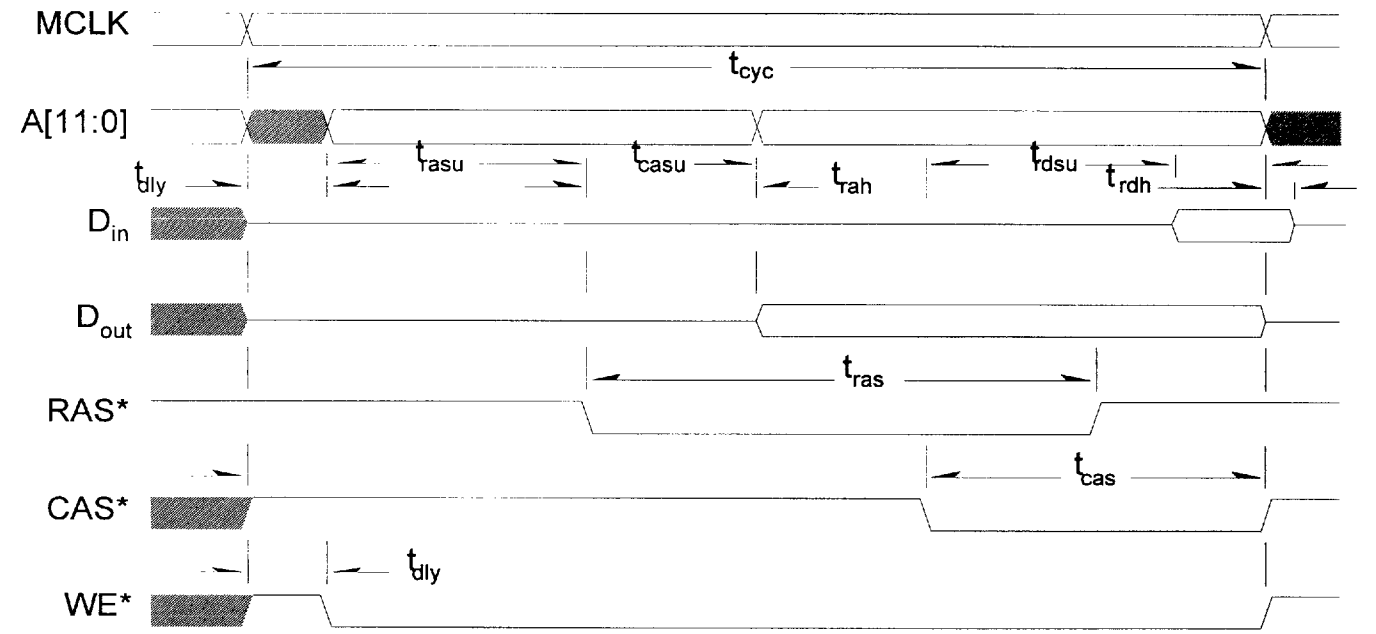
CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Memory Cycle Time	t_{cyc}	-	177	-	nSec
Memory Address/Control Delay	t_{dly}	-	15	-	nSec
Memory Read Data Setup Time	t_{rdsu}	15	-	-	nSec
Memory Read Data Hold Time	t_{rdh}	0	-	-	nSec
RAS* Active Time	t_{ras}	-	88	-	nSec
CAS* Active Delay Time	t_{cdly}	-	29	-	nSec
CAS* Active Time	t_{cas}	-	59	-	nSec
Row Address Setup Time	t_{oz}	-	44	-	nSec
Row Address Hold Time	t_{out}	-	29	-	nSec
Column Address Setup Time	t_{out}	-	29	-	nSec
Oscillator Frequency	f_{osc}			16.9344	MHz

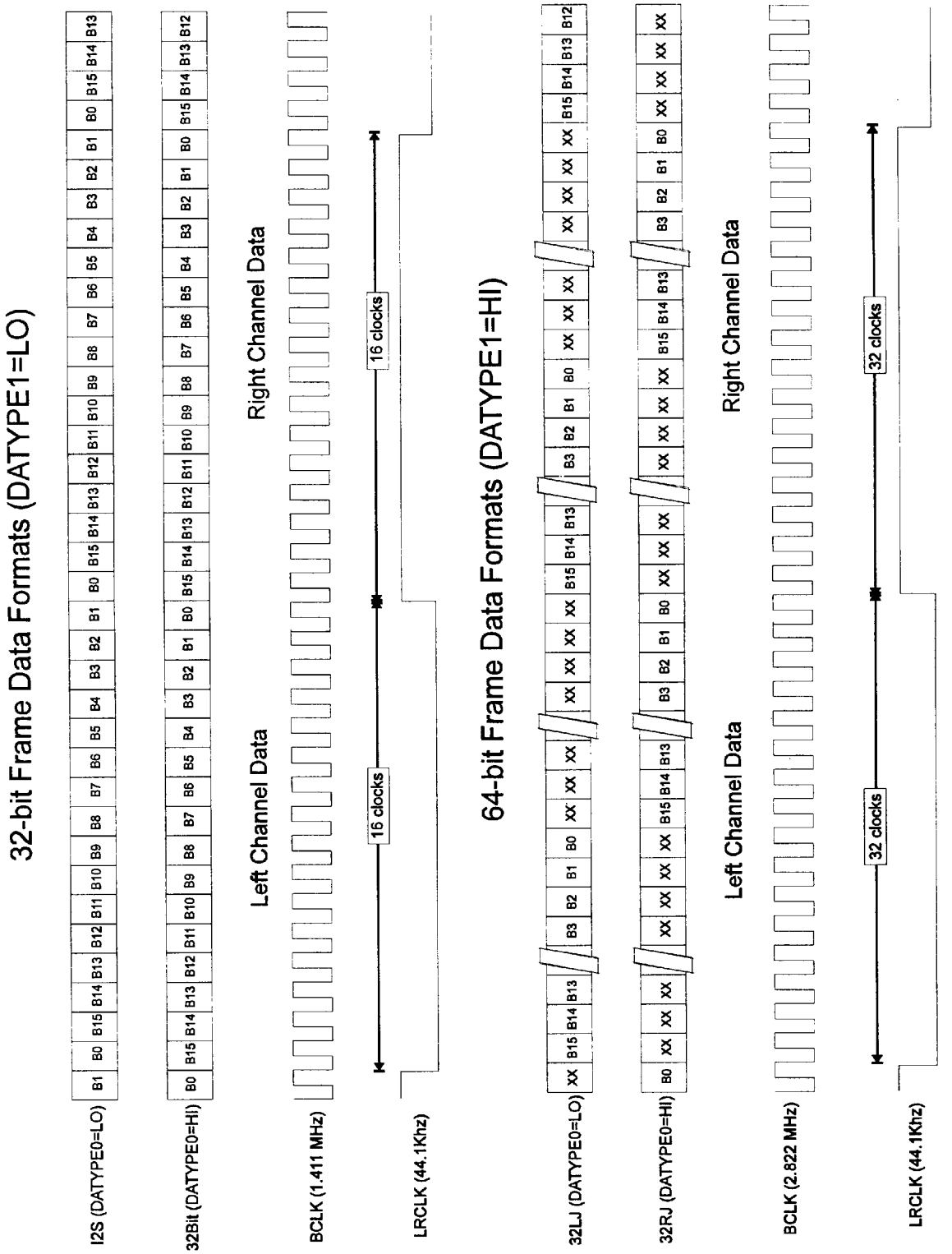
Notes:
1. Test Condition: V_{DD}=5.0V, V_{SS}=0V, f_{OSC}=16.9344MHz, T_a=25°C.

ROM/SRAM MEMORY INTERFACE TIMING



DRAM MEMORY INTERFACE TIMING





AUDIO BOARD DESIGN & PCB LAYOUT GUIDELINES

Overview

Proper analog circuit design and PCB layout are essential to achieving optimum audio performance, as well as acceptable EMI (FCC/VDE) characteristics from PC audio boards. This document outlines the basic guidelines that should be followed to ensure acceptable performance in these critical areas. As a reference, please refer to the **ΩmniWave** evaluation board schematics and PCB layout.

Design Overview

In order to achieve optimum audio performance, in terms of signal-to-noise ratio, noise, floor, and distortion, always provide separate analog and digital supplies and grounds. All digital components should be connected to power and ground, directly from the PC bus connectors. Single-ended analog circuitry, such as D/A converters, codecs, etc., should be operated from a separate +5V supply which is locally regulated down from the +12V supply available on the PC bus. All operational amplifiers should be powered by filtered +/-12V supplies derived from the +/-12V supplies available on the PC bus. Operational amplifiers should ***never*** be operated from a single-ended supply. This will not only reduce the dynamic range and headroom, but also significantly degrade the signal-to-noise ratio.

Handling Grounds

For optimum audio performance, it would be most desirable to keep the analog and digital supplies and returns totally isolated from one another. However, for the sake of EMI (FCC) performance, it is generally necessary to keep all supplies closely coupled. Also, in a PC, there are a limited number of supplies to work from, and only a single ground. These conflicting requirements are best met by allowing the digital and analog returns (VSS & VSSA) to be directly connected at only a single location, preferably directly adjacent to the card bracket. This single connection should be a substantial one, at least 100-200 mils. This connection is indicated in the Evaluation Board Schematics as a GNDSTRAP component. AC coupling the returns by means of 1-10nF capacitors straddling the perimeter of the VSSA/VSS planes, at intervals of no more than 1-1.5", should provide the coupling necessary to prevent EMI problems which can be caused by the separate ground planes. The DB-15 connector shell must be securely connected to the VSS plane, and the connector must be securely screwed to the bottom of the bracket, while the top of the bracket should have a tab which is securely screwed or riveted to the VSSA plane, thus referencing all outgoing signal lines to the (relatively) clean chassis ground at the bracket. In past designs, these techniques have consistently resulted in a >10dB margin relative to the FCC Class-B limits.

In the analog section, it is desirable to have two VSSA planes, rather than a single VSSA plane, and a single power plane. All analog supplies can be easily routed as normal traces, since the currents are very low. If possible, place the VSSA planes on the outer layers, and do all signal and power routing on the two inner layers, to minimize noise pickup from adjacent boards. In SMT designs, make layers 2 & 4 VSSA planes, and place as much routing as possible on layer 3, minimizing exposed routing on layer 1.

The VSSA plane should completely underlie **all** analog circuitry, including and D/A or A/D converters or codecs. There should be **no** power or ground routing, or unecessary digital signal routing through the area covered by the VSSA plane.

Analog Signal Routing

Proper component placement is essential to getting optimum audio performance. All traces should be kept as short and straight as possible. Avoid running traces parallel to other traces for other than very short distances. Keep any digital or clock traces as far as possible from A/D and D/A converters.

To minimize noise pickup, all routing to op-amp inputs should be kept as short as possible. Op-amp output signals are far less critical, being driven by a relatively low impedance source. Avoid routing op-amp input and output signals near each other to prevent feedback problems. Also, be sure to follow the supply bypassing guidelines below. Never route an analog signal through a digital area, or vice-versa.

Digital Signal Routing

Use of vias should be minimized, particularly on high speed signals, such as clocks. For this reason, hand-routing is **strongly** recommended, rather than using an autorouter. Even the best auto-routers available today will use far more vias than an experienced hand-router. Our evaluation boards are all completely hand-routed. Keep all un-buffered PC-bus signals as short as possible, preferably no more than 1-2". Also rigorously avoid passing digital signals over any splits in the planes. Keep all crystals as close as possible to the other components to which they are connected, and, if possible, surround their traces with VSS traces. **Never** allow an oscillator or clock signal to cross the VSS/VSSA plane split! Securely attach, by soldering, the crystal case to its associated ground plane, usually VSS.

Supply Bypassing

In the digital section of the board, be sure no VDD pin is more than about 1" from a bypass capacitor. In the analog section, this may be relaxed somewhat, but try to ensure that each supply pin is within at least 1.5-2" of a bypass capacitor. In both the digital and analog sections, evenly distribute the bypass capacitors, and use an even mix of .1uF and .001 uF capacitors. For the ΩmniWave chip, one bypass capacitor for each VDD pin is recommended. All bypass capacitors should be routed such that the connection is from the VDD and VSS planes to the capacitor, and then from the capacitor to the IC pins.

EMI Suppression

Adequate EMI suppression can most easily be achieved through careful PCB layout, and the use of small capacitors to VSS/VSSA, rather than ferrite beads. Since the analog input and output signal points are all (relatively) low impedance, small capacitors (1-10nF) can be connected between these points and VSSA with no appreciable effect on audio performance. All such capacitors should be placed as close as possible to the connectors, and the traces leaving them (going to the connectors) should not pass near any un-filtered traces which might couple-in unwanted high-frequency noise.

PACKAGE DIMENSIONS (100-QFP-1420C)